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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,828	03/15/2004	Chien-Ting Lai		3134

25859 7590 05/04/2005

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EXAMINER	
DOAN, THERESA T	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/801,828	LAI ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The corrected drawing filed on 02/28/05 is approved.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 6, 8 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Denton et al. ("Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate", IEEE Electron Device Letters, Vol. 17, No. 11, November 1996, pgs. 509-511).

Regarding claims 1 and 8, Denton (figure 1) discloses a thin film transistor, comprising:

a substrate (figure 1a);

a gate electrode disposed in the substrate (polysilicon bottom gate, see figure 1a);

a gate insulation layer (SiO_2, see figure 1a) disposed on the substrate and gate electrode (see figure 1a);

a channel layer disposed on the gate insulation layer (see figure 1c);

a source/drain ohmic contact layer arranged on opposite ends of the channel layer (see figure 1c);

a source electrode disposed on the substrate and source ohmic contact layer (figure 1c); and

a drain electrode disposed on the substrate and drain ohmic contact layer (figure 1c).

Regarding claim 2, Denton (figure 1) discloses the surface of the gate electrode is parallel with the surface of the substrate.

Regarding claim 6, Denton (figure 1) discloses wherein a cross-section of the gate electrode is rectangular.

Regarding claim 21, Denton (figure 1) discloses a thin film transistor, comprising:

a substrate defining a cavity in an upper face thereof (figure 1a);

a gate electrode filled in the cavity (polysilicon bottom gate, see figure 1a);

a gate insulation layer (SiO_2, see figure 1a) applied upon the substrate and gate electrode (see figure 1a);

a channel layer applied upon the gate insulation layer and only covering a central portion of an upper face of the gate insulation layer (see figure 1c);

a source/drain ohmic contact layer arranged on opposite ends of the channel layer (see figure 1c);

a source electrode disposed upon one side of the channel layer and further covering a portion of the gate insulation layer wherein the portion is exposed to an exterior before the source electrode is applied thereto (figure 1a); and

a drain electrode disposed upon the other side of the channel layer and further covering another portion of the gate insulation layer wherein another portion is exposed to the exterior before the drain electrode is applied thereto (figure 1a).

It is noted that the process limitation (exposed before) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

4. Claims 1-2 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Maeda (U.S Pat. 6,423,578).

Regarding claim 1, Maeda (figure 9) discloses a thin film transistor, comprising:

a substrate 50a (figure 9);

a gate electrode 41 disposed in the substrate 50a;

a gate insulation layer 40 disposed on the substrate and gate electrode (see figure 9);

a channel layer disposed on the gate insulation layer 40 (see figure 9);

a source/drain ohmic contact layer (E/D) arranged on opposite ends of the channel layer (see figure 9);

a source electrode 91 disposed on the substrate 50a and source ohmic contact layer (figure 9); and

a drain electrode 92 disposed on the substrate 50a and drain ohmic contact layer (figure 9).

Regarding claim 2, Maeda (figure 9) discloses the surface of the gate electrode 41 is parallel with the surface of the substrate 50a.

Regarding claim 6, Maeda (figure 9) discloses wherein a cross-section of the gate electrode is rectangular.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda (U.S Pat. 6,423,578).

Maeda (figure 9) discloses that the substrate 50a is an insulating layer, but does not disclose that the insulating layer 50a is made of silicon oxide.

However, it would have been obvious to form the insulating layer 50a with silicon oxide because the silicon oxide material has an insulating characteristic and is well known and commonly used in the art for providing the isolation.

7. Claims 3-5 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denton et al. in view of Hiramatsu et al. (U.S. Pat. 5,311,040).

Regarding claims 3-4, Denton does not disclose the gate electrode is made of metallic material comprising Cu, Al, Ti, Mo, Cr, Ta or Nd.

However, Hiramatsu discloses (figure 1) a gate electrode 2, which is made of Ta or MoTa (column 3, lines 25-26) in order to increase conductivity of the semiconductor gate electrode. Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the metallic gate electrode as set forth above because as taught by Hiramatsu, such the metallic gate electrode would increase the conductivity of the semiconductor gate electrode.

Regarding claim 5, Denton does not disclose wherein the cross-section of the gate electrode is trapezoidal.

However, Hiramatsu (figure 1) discloses wherein the cross-section of the gate electrode 2 is trapezoidal. Accordingly, it would have been obvious to form different shapes of the gate electrode in Denton's structure as taught by Hiramatsu, because such changing shapes of gate electrode are not critical and would provide the same results. Applicant can rebut a prima facie case of obviousness based on ranges by showing unexpected results or the criticality of the claimed. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claim. In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves

unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP 716.02 - 716.02(g) for a discussion of criticality and unexpected results. There is nothing in the present application to indicate that the gate electrode's shapes are critical.

Regarding claims 9-10, Denton (figure 1) discloses a silicon epitaxial lateral over growth (see Introduction), wherein the source and drain ohmic layers are formed by doping the channel layer but does not show the silicon channel layer is made of amorphous silicon or polycrystalline silicon. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form amorphous silicon or polycrystalline silicon for channel layer in Denton's device, because it is well known within the skills of an artisan to form amorphous silicon or polycrystalline silicon for channel layer in order to increase the conductivity in the thin film transistor.

8. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denton et al. in view of Honda (U.S. Pat. 6,639,246).

Denton (figure 1) discloses a thin film transistor comprising:

a substrate (figure 1a);

a gate electrode disposed in the substrate (polysilicon bottom gate, see figure 1a);

a gate insulation layer (SiO_2, see figure 1a) disposed on the substrate and gate electrode (see figure 1a);

a channel layer disposed on the gate insulation layer (see figure 1c);

a source/drain ohmic contact layer arranged on two sides of the channel layer (see figure 1c);

a source electrode disposed on the substrate and source ohmic contact layer (figure 1c); and

a drain electrode disposed on the substrate and drain ohmic contact layer (figure 1c).

Denton does not disclose that the thin film transistor is used in a display device.

However, Honda (figure 9) discloses a display device including a plurality of thin film transistors used to control and drive display material, wherein the display material is liquid crystal (figure 9, column 12, lines 11-21). Accordingly, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply a thin film transistor of Denton in a display device including a plurality of thin film transistors used to control and drive display material because as taught by Honda, such a display device including a plurality of thin film transistors would provide an active matrix type liquid crystal display (column 12, lines 12-13). The recitation of using "a display device including a plurality of thin film transistors used to control and drive display material" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190

USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Response to Arguments

Applicant's arguments with respect to claims 1-12 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
April 26, 2005.

PHAT X. CAO
PRIMARY EXAMINER

Replacement Sheet

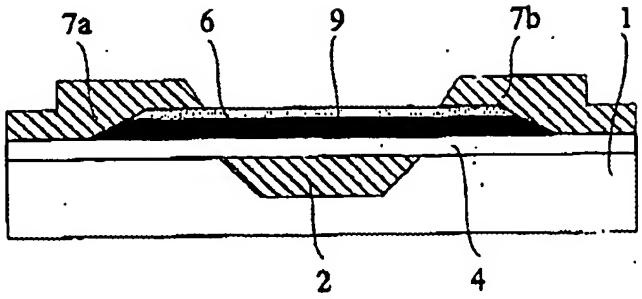

FIG. 13

Approved TO 04/25/05

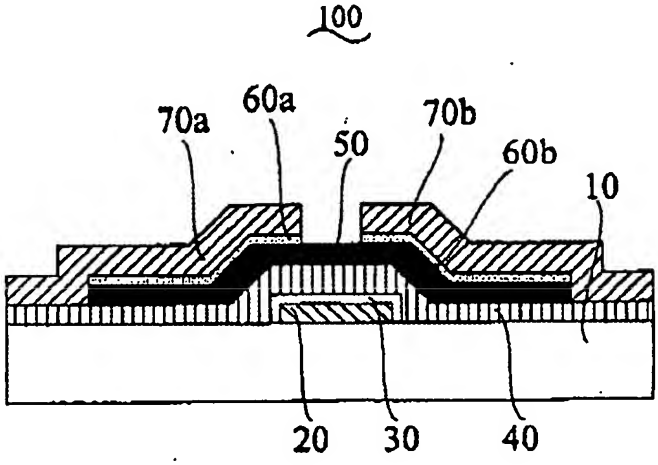

FIG. 14

(PRIOR ART)